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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,919	03/02/2004	Ta-Lee Yu	TS2000068BD	1400

7590 07/27/2004

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,919	YU, TA-LEE	
	Examiner	Art Unit	
	Theresa T Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/02/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-29 and 31* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 25-31 are objected to because of the following informalities:

In claims 25-26, change "**dopent**" to - -**dopant**- - throughout entire claims.

In claim 25, line 14, change "." to - - ; - -. And line 16 change "," to "." .

In claims 25-31, Applicant needs to keep element recitations consistent for clarity. For example, in claim 25, line 7, Applicant uses term "third semiconductor layer" to define an element and in claim 27, line 2, Applicant uses term "third semiconductor **base** layer" to refer to the same element.

In claim 27, line 1, change "**said** laterally spaced" to --**a** laterally spaced--.

In claim 28, line 1, change "**said** first collector regions" to - -**a** first collector regions- -.

In claim 29, line 1, change "**said** array" to - -**an** array- -. And also in line 1 "...a **said** contact" deletes "**said**".

In claim 29, line 2, change "**said** emitter contact region" to - -**an** emitter contact region- -. And also in line 2 "...a **said** contact" deletes "**said**".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 26, line 3, the limitation of "**the bases** are formed by **said** third conductivity layer..." is unclear because the location of the bases formed by a third conductive layer is unknown.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 25-29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (U.S. Pat. 5,850,095) of record.

Regarding claims 25-26, Chen et al. discloses (in figure 4) an integrated multiple vertical npn transistor ESD protection structure (40) on a semiconductor substrate (42), functionally connected to an integrated circuit pin (34) which will prevent electrostatic discharge damage to the integrated circuit comprising: a first semiconductor layer (44) having a first conductivity dopant type (n+ layer); a second semiconductor layer (46; n-type) overlying the first semiconductor layer, having a similar conductivity type as the first layer, but a different dopant concentration; a third semiconductor layer (62) having a second conductivity

dopant type (p-type), disposed in overlying relation to the second semiconductor layer; a plurality of first regions (50) of the first conductivity type (n+) electrically connecting with the first semiconductor layer, having a top element making electrical contact (58) to the first regions and the first semiconductor layer; a plurality of second regions (56/64) of the second conductivity dopent type (p-type) laterally spaced from the first regions, being electrically connected to the third semiconductor layer having a top element making electrical contact (74) to the second regions and the second semiconductor layer; a plurality of third regions (66) of the first semiconductor layer (n+regions) laterally spaced and interposed between the second regions (column 3, line 27 to column 4, line 64).

Regarding claims 28 and 31, Chen (figures 4-5) discloses the first regions (50) have horizontal contact conductor stripes at the top and bottom of the transistor array which are ultimately connected together and to a first voltage source of the integrated circuit pin (34) (column 3, line 27 - column 4, line 64).

Regarding claims 27 and 29, Chen (figures 4-5) discloses an array comprises a contact and an emitter contact region (68), and the second semiconductor horizontal contact region (74) between the bottom horizontal collector contact and a "N"' number of the n doped third semiconductor emitter regions (62) whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise the ESD protection structure.

Allowable Subject Matter

6. Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose all the combination of an integrated multiple npn transistor ESD protection structure comprising the third semiconductor emitter regions are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous comb like manner by a vertical contact conductor element at one end of said horizontal emitter conductor stripes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Thursday from 8:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
July 22, 2004.

PHAT X. CAO
PRIMARY EXAMINER